|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Net name** | **U1 FPGA Pin (LOC)** | **J20 connector Pin** | **J63 FMC LPC Pin** | **Schematic NET name** |
| PH1 | P29 | 1 | G21 | FMC\_LPC\_LA20\_P |
| PH2 | N32 | 2 | H28 | FMC\_LPC\_LA24\_P |
| SO\_not\_Up | R29 | 3 | G22 | FMC\_LPC\_LA20\_N |
| SO\_Up | P32 | 4 | H29 | FMC\_LPC\_LA24\_N |
| SO\_not\_Down | R26 | 5 | H25 | FMC\_LPC\_LA21\_P |
| SO\_Down | P31 | 6 | G27 | FMC\_LPC\_LA25\_P |
| CAout | T26 | 7 | H26 | FMC\_LPC\_LA21\_N |
| CBout | P30 | 8 | G28 | FMC\_LPC\_LA25\_N |
| CA\_SI | N27 | 9 | G24 | FMC\_LPC\_LA22\_P |
| CB\_SI | L33 | 10 | D26 | FMC\_LPC\_LA26\_P |
| OutEn | P27 | 11 | G25 | FMC\_LPC\_LA22\_N |
| Ph\_En | M32 | 12 | D27 | FMC\_LPC\_LA26\_N |
| Trig | R28 | 13 | D23 | FMC\_LPC\_LA23\_P |
| SO\_not\_Up\_In | R31 | 14 | C26 | FMC\_LPC\_LA27\_P |
| SO\_Up\_In | R27 | 15 | D24 | FMC\_LPC\_LA23\_N |
| SO\_not\_Down\_In | R32 | 16 | C27 | FMC\_LPC\_LA27\_N |
| SO\_Down\_In | N33 | 5 (J16) | H31 | FMC\_LPC\_LA28\_P |